The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. **(Withdrawn)** A conductive memory device comprising:

a bottom electrode having a top face and ;

a top electrode located above the bottom electrode having a bottom face; and

a multi-resistive state element sandwiched between the bottom electrode and the top electrode and having a bottom face and a top face, the multi-resistive state element's bottom face being in contact with the bottom electrode's top face, and the multi-resistive state element's top face being in contact with the top electrode's bottom face;

wherein the bottom electrode, the top electrode and the multi-resistive state element each have sides that are adjacent to their faces; and

wherein the sides are at least partially covered by a sidewall layer.

2. **(Withdrawn)** The conductive memory device of claim 1 wherein the sidewall layer is a diffusion barrier.

3. **(Withdrawn)** The conductive memory device of claim 2 wherein the diffusion barrier is also an etch stop.

4. **(Withdrawn)** The conductive memory device of claim 2 wherein the diffusion barrier is $Si_3N_4$, $TiO_2$ or $Al_2O_3$.

5. **(Withdrawn)** The conductive memory device of claim 1 wherein:

the bottom electrode's top face has a first surface area;

the multi-resistive state element's bottom face has a third surface area; and

the first surface area is larger than the third surface area.

6. **(Withdrawn)** The conductive memory device of claim 1 wherein:

the top electrode's bottom face has a second surface area;

the multi-resistive state element's top face has a fourth surface area; and

the second surface area is larger than the fourth surface area.

7. **(Withdrawn)** The conductive memory device of claim 1 wherein:

the top electrode's bottom face has a second surface area;

the multi-resistive state element's top face has a fourth surface area; and

the second surface area is smaller than the fourth surface area.

8. **(Withdrawn)** The conductive memory device of claim 7 further comprising:

a hard mask layer having a bottom face with a surface area substantially similar to the second surface area;

wherein the top electrode has a top face that is in contact with the bottom face of the hard mask layer.

9. **(Withdrawn)** The conductive memory device of claim 1 wherein:

the bottom electrode's top face has a first surface area;

the top electrode's bottom face has a second surface area;

the multi-resistive state element's bottom face has a third surface area;

the multi-resistive state element's top face has a fourth surface area; and

the first, second, third and fourth surface areas are approximately equal.

10. **(Withdrawn)** The conductive memory device of claim 9 wherein the bottom electrode's top face, the top electrodes bottom face, the multi-resistive state element's bottom face and the multi-resistive state element's top face are substantially aligned, thereby all the faces have the same footprint.

11. **(Withdrawn)** The conductive memory device of claim 1 wherein, expressed in an X-Y-Z Cartesian coordinate system:

the top and bottom faces of the bottom electrode, the top electrode and the multi-resistive state element lie essentially in the X-Y plane; and

the direction of current conduction through the conductive memory device is essentially parallel to the Z-axis.

12. **(Cancelled)**

13. (**Currently Amended**) A method of making an integrated circuit comprising:

providing **a** semiconductor wafer **including active circuitry previously fabricated on the semiconductor wafer** ;

performing front end of line (FEOL) processes on the semiconductor wafer;

forming a plurality of conductive memory devices **[[ , ]]** atop **the active circuitry on** the **FEOL** processed semiconductor wafer, each conductive memory device operable to be reversibly placed in multiple resistive states;

forming a sidewall layer around the plurality of conductive memory devices; and conducting metallizations after the plurality of conductive memory devices are formed.

14. (Original) The method of making an integrated circuit of claim 13 further comprising annealing after the plurality of conductive memory devices are formed.

15. (Original) The method of making an integrated circuit of claim 13 wherein the FEOL processes include the formation of a first inter-layer dielectric.

16. (Original) The method of making an integrated circuit of claim 15 wherein each conductive memory device is a memory plug including a bottom electrode, a top electrode located above the bottom electrode and a multi-resistive state element sandwiched between the bottom electrode and the top electrode.

17. (Original) The method of making an integrated circuit of claim 16 further comprising:

forming a plurality of contact holes prior to the formation of a plurality of conductive memory devices, each contact hole corresponding to the location of a conductive memory plug, through the first inter-layer dielectric; and

depositing a conductive material within the contact holes.

18. (Original) The method of making an integrated circuit of claim 17 further comprising, between depositing the conductive material within the contact holes and depositing the conductive plug material, forming a barrier/adhesion layer.

19. (Original) The method of making an integrated circuit of claim 17 wherein:

each contact hole has a top surface area;

each conductive memory device has a bottom surface area that is larger than the contact hole's top surface area such that each conductive memory device has an overhang that is not in contact with the contact hole's top surface area; and

a barrier layer is in contact with the plug's overhang.

20. (Previously Presented) The method of making an integrated circuit of claim 13 further comprising conducting a first metallization before the plurality of conductive memory devices are formed.

21. **(Cancelled)**

22. (Previously Presented) A method of making a plurality of conductive memory devices, each conductive memory device operable to be reversibly placed in multiple resistive states, the method comprising:

sputtering a bottom electrode layer;

sputtering a multi-resistive state element layer;

sputtering a top electrode layer;

modifying an interface property between the multi-resistive state element layer and the top electrode layer; and

photo lithographically patterning the top electrode.

23. (Original) The method of making a plurality of conductive memory devices of claim 22 wherein modification of the interface performed by either ion implantation, in situ argon plasma treatment, in situ oxygen plasma treatment, in situ annealing in argon or in situ annealing in oxygen.

24. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 wherein at least one of the sputtering process of sputtering the bottom electrode layer, sputtering the multi-resistive state element layer or sputtering the top electrode layer uses an off-axis sputtering technique.

25. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 wherein at least two consecutive sputtering processes of sputtering the bottom electrode layer, sputtering the multi-resistive state element layer or sputtering the top electrode layer use a continuous deposition technique.

26. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 wherein the multi-resistive state element sputtering process uses a co-sputtering deposition technique.

27. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 further comprising

wet etching the multi-resistive state element; and

wherein the wet etching is performed after the patterning, the patterning forming top electrode sides, bottom electrode sides and multi-resistive state element sides.

28. (Original) The method of making a plurality of conductive memory devices of claim 27 wherein the wet etching of the multi-resistive state element removes a thickness of 50 - 150 Å, thereby forming an undercut so as to remove process-induced material defects from the multi-resistive state element's sides.

29. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 further comprising high temperature reactive ion etching of the electrode, the multi-resistive state element and the bottom electrode after photo lithographically patterning the top electrode.

30. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 wherein at least one of the bottom electrodes and the top electrodes include a conductive layer and a barrier layer to prevent metal inter-diffusion.

31. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 wherein sputtering the multi-resistive state element layer is carried out at less than or equal to about 600°C.

32. (Previously Presented) The method of making a plurality of conductive memory devices of claim 22 further comprising depositing an etch stop/diffusion barrier.

33. (Original) The method of making a plurality of conductive memory devices of claim 32 further comprising:

etching the electrode, the multi-resistive state element and the bottom electrode in order to create a patterned stack after photo lithographically patterning the top electrode;

depositing a second inter-layer dielectric;

planarizing the second inter-layer dielectric by chemical-mechanical polishing; and

forming a plurality of via holes, locationally and geometrically corresponding to the top electrodes of the conductive memory devices, with photolithography and a via etch.

34. (Previously Presented) The method of making a plurality of conductive memory devices of claim 33 further comprising depositing a conductive material within the plurality of via holes.

35. (Original) The method of making a plurality of conductive memory devices of claim 34 further comprising depositing a barrier/adhesion layer on the patterned stack that includes the top electrode, multi-resistive state element and bottom electrode.

36. (Original) The method of making a plurality of conductive memory devices of claim 35 further comprising forming a plurality of conductive plugs within the formed plurality of via holes and atop the deposited barrier/adhesion layer.

37. (Original) The method of making a plurality of conductive memory devices of claim 36 further comprising conducting subsequent metallizations after the plurality of conductive plugs are formed.

38. **(Withdrawn)** A conductive memory device comprising:

a bottom electrode having a top face and ;

a top electrode located above the bottom electrode having a bottom face; and

a multi-resistive state element sandwiched between the bottom electrode and the top electrode and having a bottom face and a top face, the multi-resistive state element's bottom face being in contact with the bottom electrode's top face, and the multi-resistive state element's top face being in contact with the top electrode's bottom face;

wherein the bottom electrode, the top electrode and the multi-resistive state element each have sides that are adjacent to their faces.

39. **(Withdrawn)** The conductive memory device of claim 38 wherein:

the bottom electrode's top face has a first surface area;

the top electrode's bottom face has a second surface area;

the multi-resistive state element's bottom face has a third surface area;

the multi-resistive state element's top face has a fourth surface area; and

the first, second, third and fourth surface areas are approximately equal.

40. **(Withdrawn)** The conductive memory device of claim 39 wherein the bottom electrode's top face, the top electrodes bottom face, the multi-resistive state element's bottom face and the multi-resistive state element's top face are substantially aligned, thereby all the faces have the same footprint.